

SY2 BLOCK DIAGRAM

CPU
Atom N270/N280
437 PIN (FCBGA)
22mm x 22mm P3,4

CPU Thermal Sensor P3

CLOCK GEN
SLG8SP513VTR P2

NB
INTEL 945GSE
998PIN (FCBGA)
27mm x 27mm P5,6,7,8,9

DDRII SO-DIMM P11

533/400 MHZ
Single Channel

FSB 667/533Mhz

VGA

CRT P10
LCD P7

Battery

DC In

DC/DC & Charge P32

SB
ICH7-M
652 BGA
31mm x 31mm P12,13,14,15

USB CNN x2 P25

USBX2<PORT0-1>

Bluetooth P22

USBX1<PORT3>

Camera P7

USBX1<PORT7>

DMI x2

1X PCI-E<GPP_PORT1>

LAN 10/100 AR8132M P23

RJ-45 P23

1X PCI-E<GPP_PORT2>

Wi-LAN P16

SATA<PORT0>

2.5-inch HDD P24

PATA

SSD P24

PCI 33Mhz

32.768MHz

Ricoh R5C833 P17

MS-DUO Card P17

SD Card P17

HD Audio

Codec
ALC262 P19

Digital Mic P7

MIC-In Jack P21

HP-Out Jack P21

AMP TPA2017D2


Int. Speaker
2W x2 P20

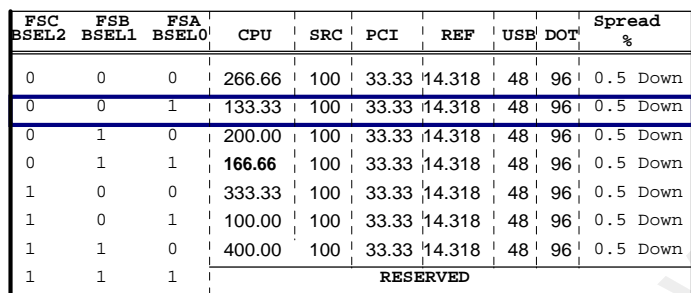
LPC 33Mhz

Touch PAD P22

PCU
WPCE775L P18
32.768MHz

BIOS
1MB FLASH P18

			
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27 Select PIN13	PIN 20/21	PIN 24/25
* 0	DOT_96 / DOT_96#	LCDCCLK / LCDCCLK#
1	SRC_0 / SRC_0#	27M / 27M_SS

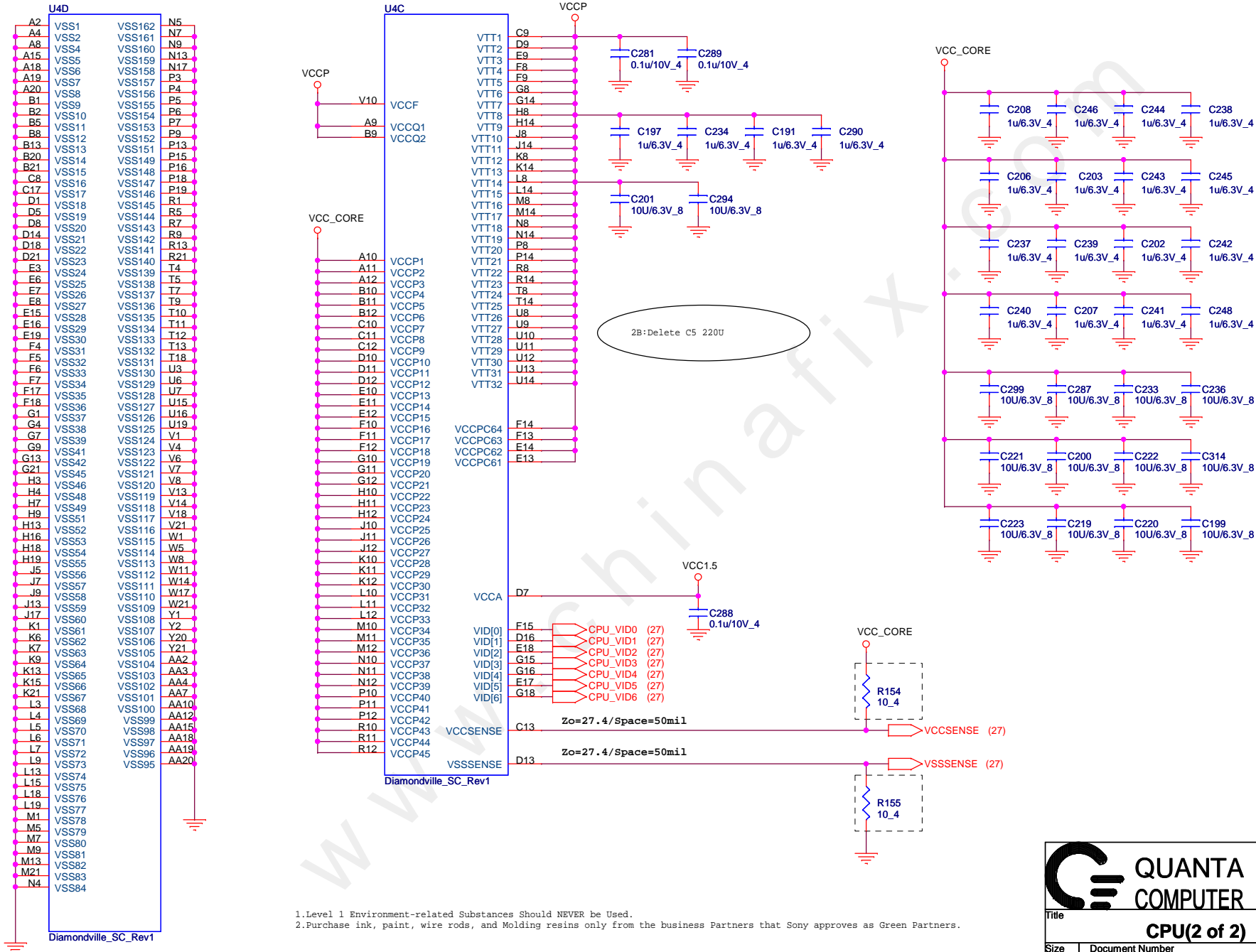
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ITP_EN(PIN14)	PIN53/54
* 0	SRC8#/SRC8
1	ITP/ITP#

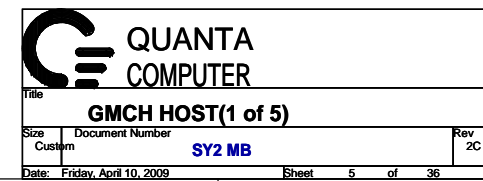


Title	CLKGEN
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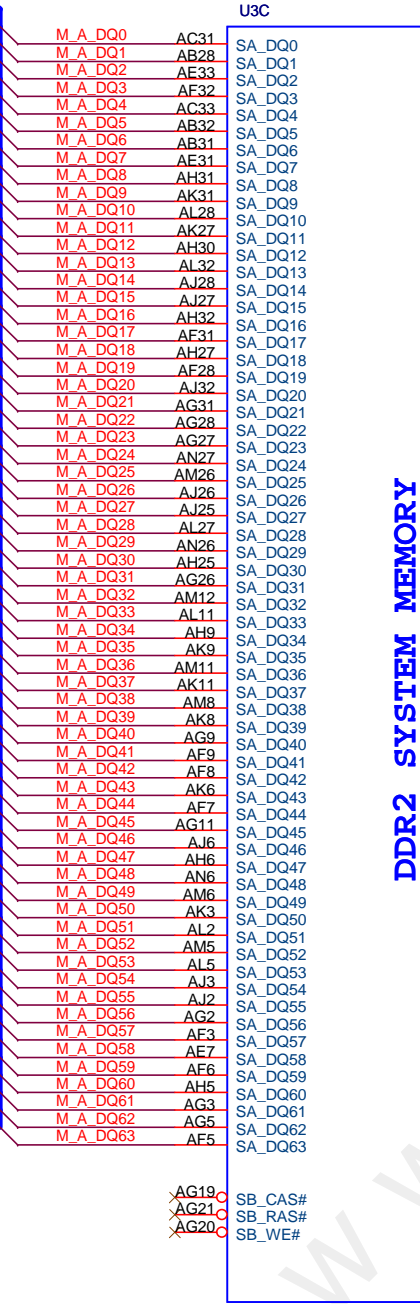
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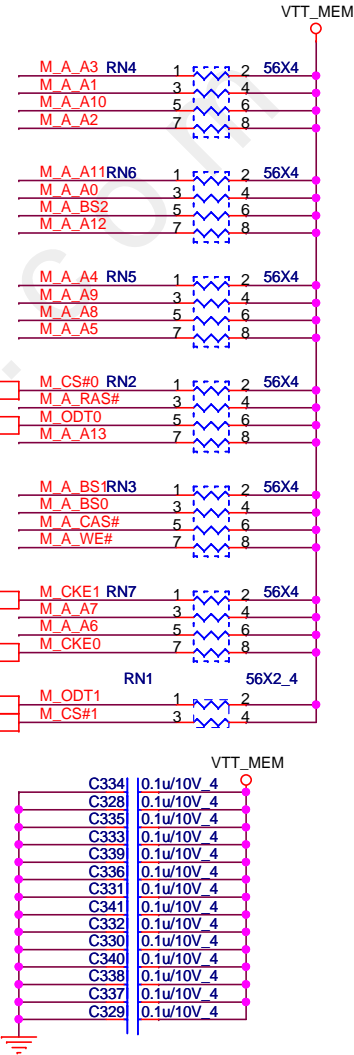
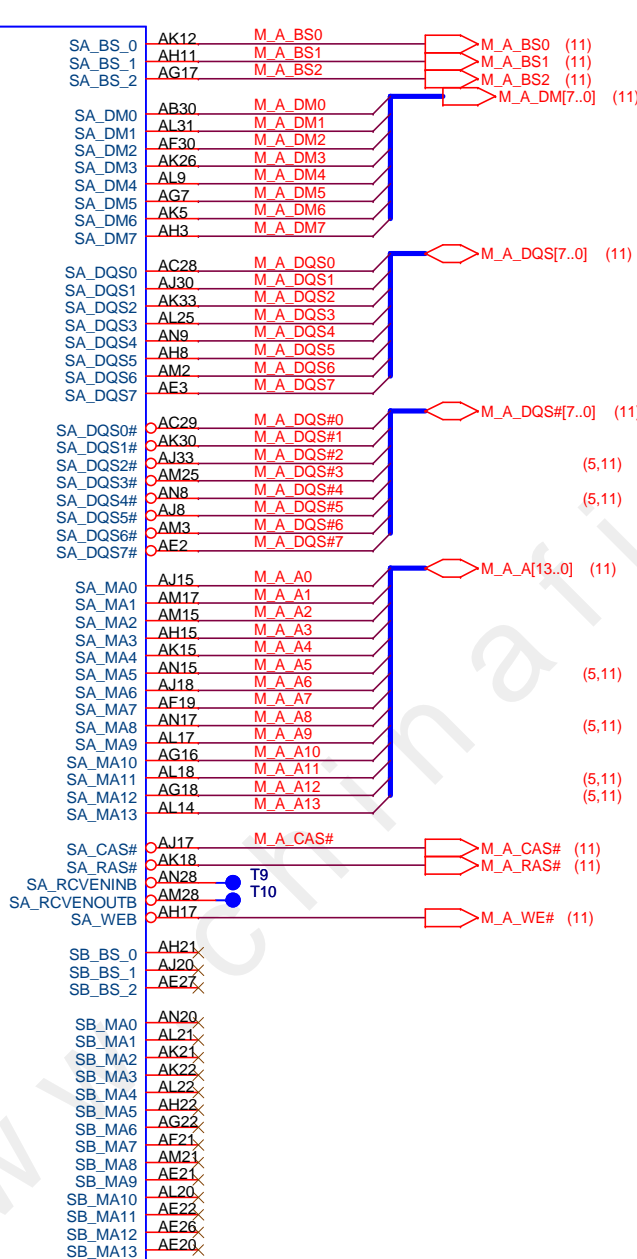
		QUANTA COMPUTER	
		CPU(2 of 2)	
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(11) M_A_DQ[63..0]

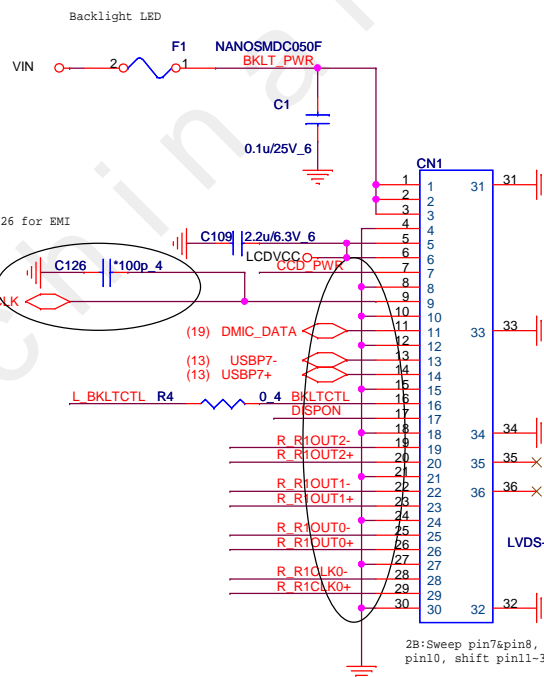
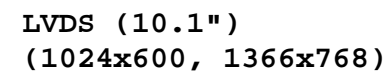
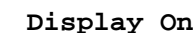
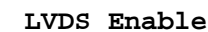


945GSE



		<p>QUANTA COMPUTER</p>	
		<p>Title</p>	
<p>Size</p>		<p>Document Number</p>	
<p>Custom</p>		<p>SY2 MB</p>	
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<p>Rev 2C</p>		<p>GMCH DDR (2 of 5)</p>	

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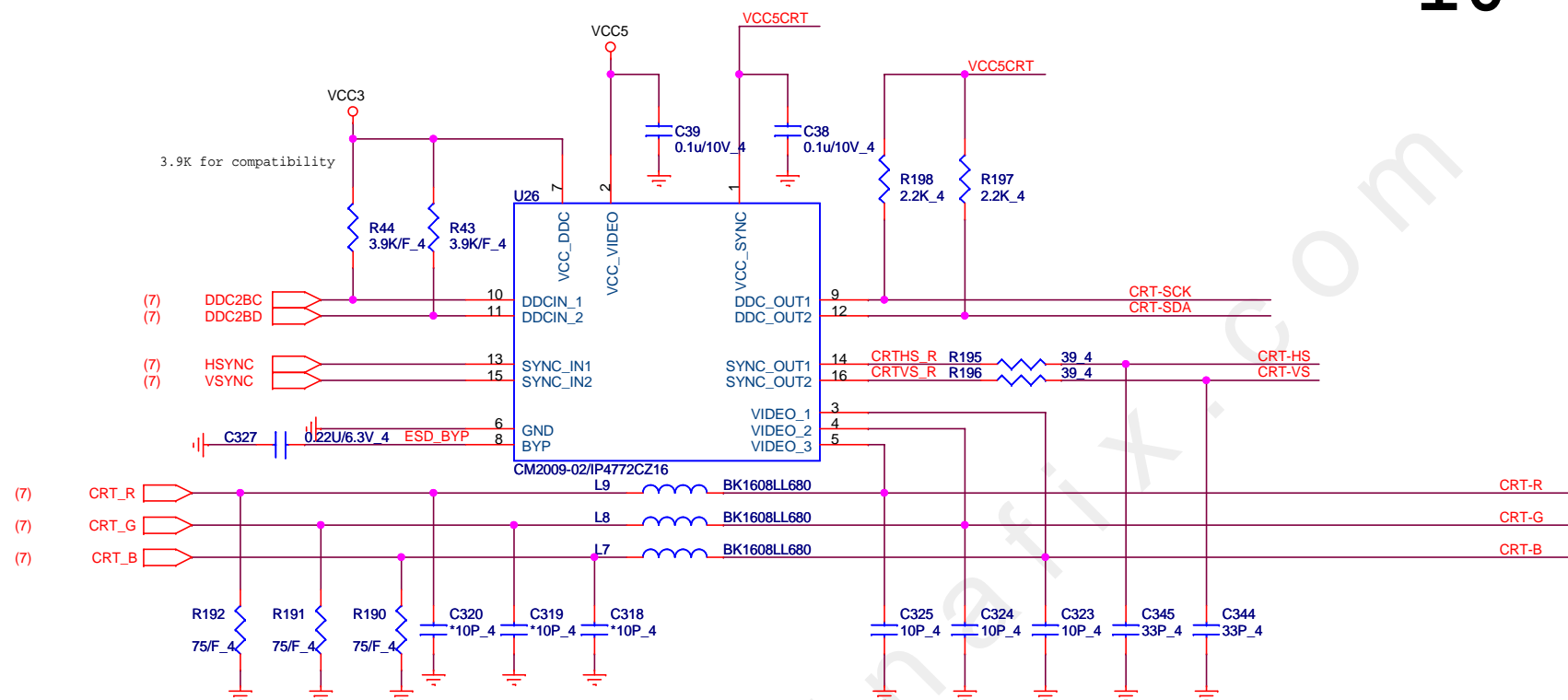
Size	Document Number
Custom	SY2 MB

Rev	2C
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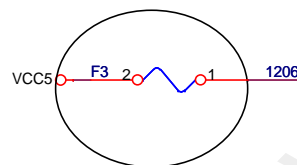
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Title			
GMCH Power 2 (4 of 5)			
Size	Document Number	Rev	
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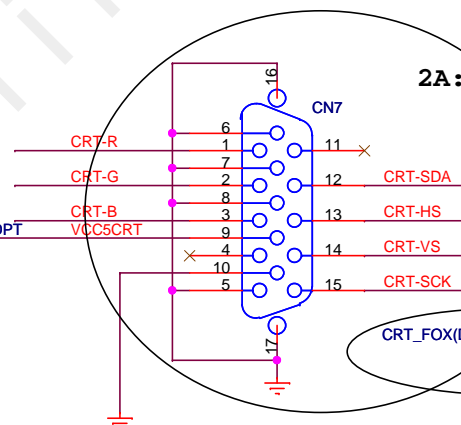


VCC5CRT(5V+-10%)
Current limit <1A



2A: Change F3 to 0.25A ((hold))


2A: Correct PCB-FP symbol

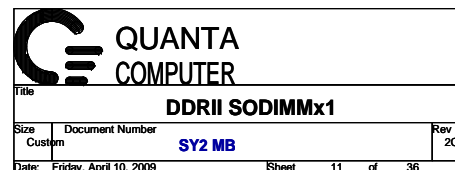


2A: Change CRT CN in gray color(new p/n)

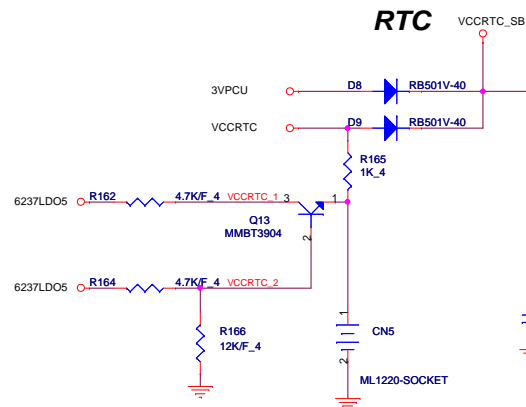
CRT_FOX(DZ11A01-NA205-9F)

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Title		
CRT		
Size	Document Number	Rev
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2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



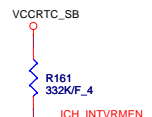
ML1220 cell
AHL03014003

XOR Chain Entrance Strap PCIE Port configuration

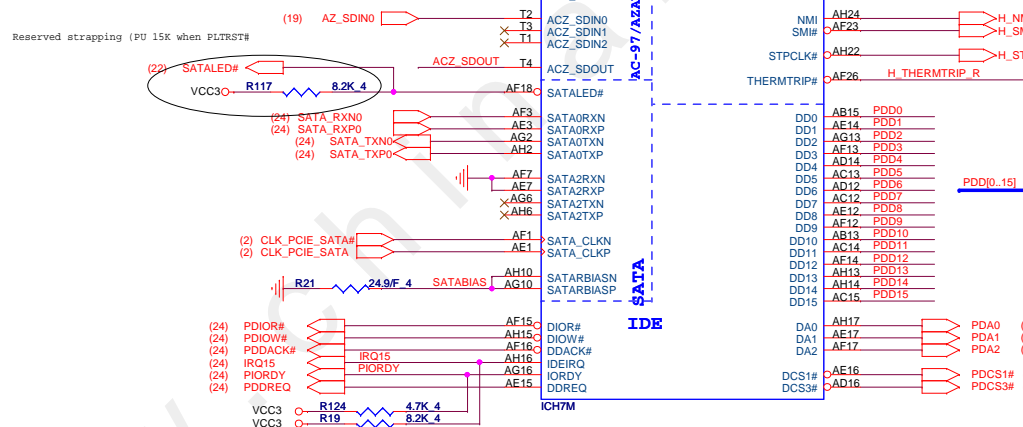
ICH_TP3 (INT PU)	ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0		RSVD
0	1		Enter XOR Chain
1	0	0	* Normal operation 4 x 1s
1	1	1	PCIE Port1 (4x)

Internal VRM Enable for Vccsus1_05

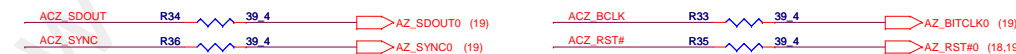
	INTVRMEN
Enable (default)	1
Disable	0



Reserved strapping (PU 15K when PLTRST#)

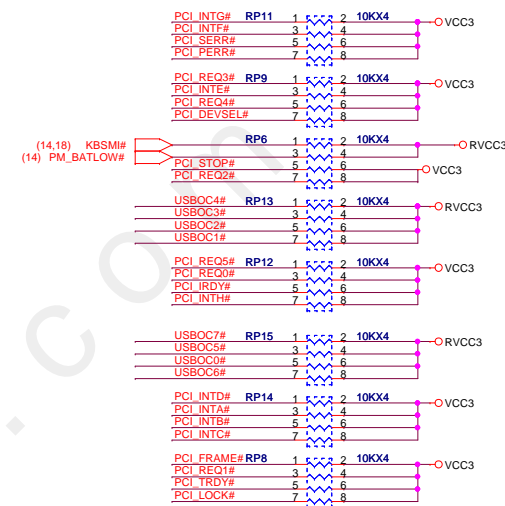


HD to Audio Codec



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QUANTA COMPUTER	
Title: ICH9-M HOST(1 of 4)	
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A16 SWAP Override strap	
PCI_GNT#3	Low = A16 swap override enabled High = Default

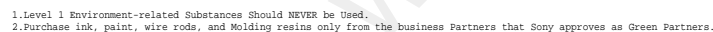
PCI_GNT#5 (INT PU)	PCI_GNT#4 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	PCI (Default)

IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2



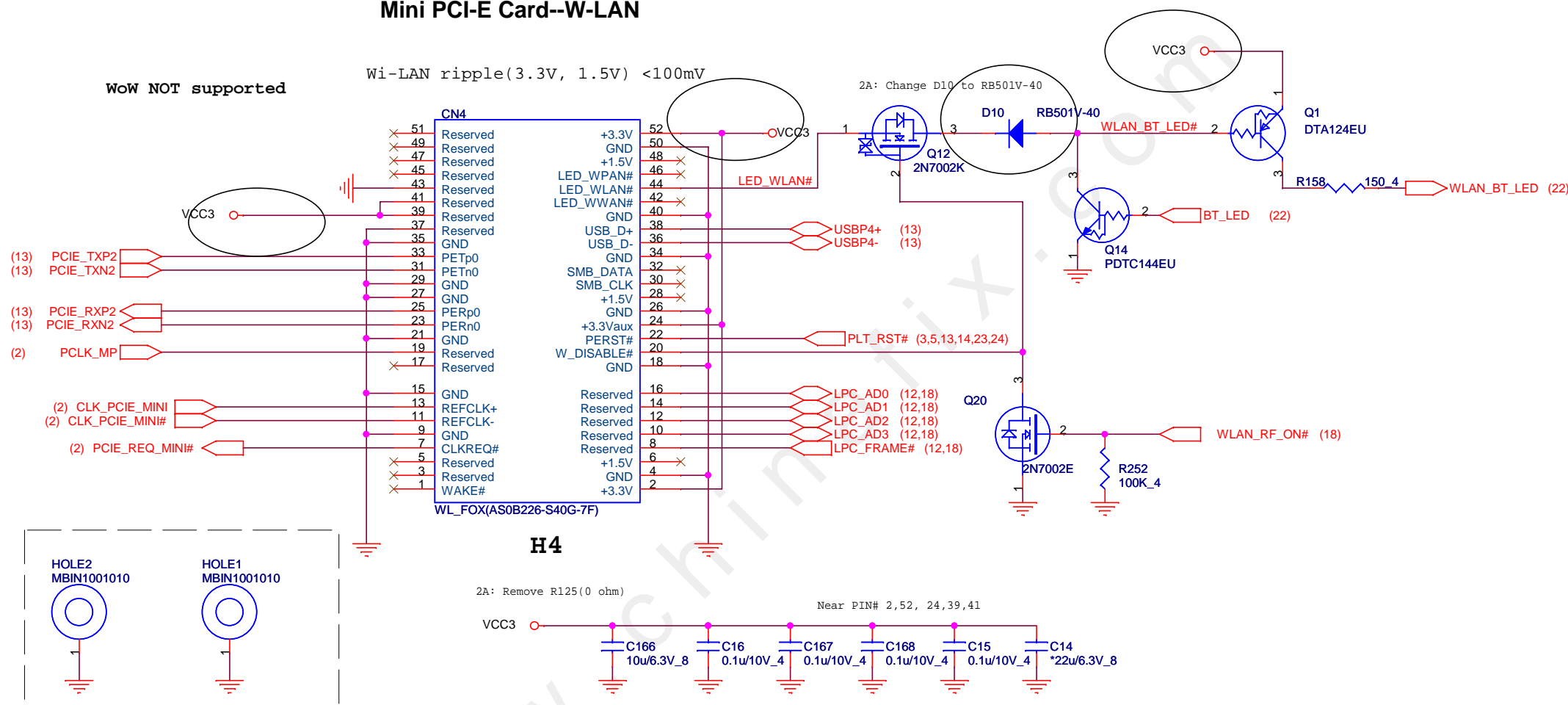
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WoW NOT supported

Wi-LAN ripple(3.3V, 1.5V) <100mV



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Title

WLAN & BT

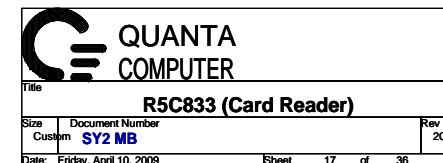
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Custom	

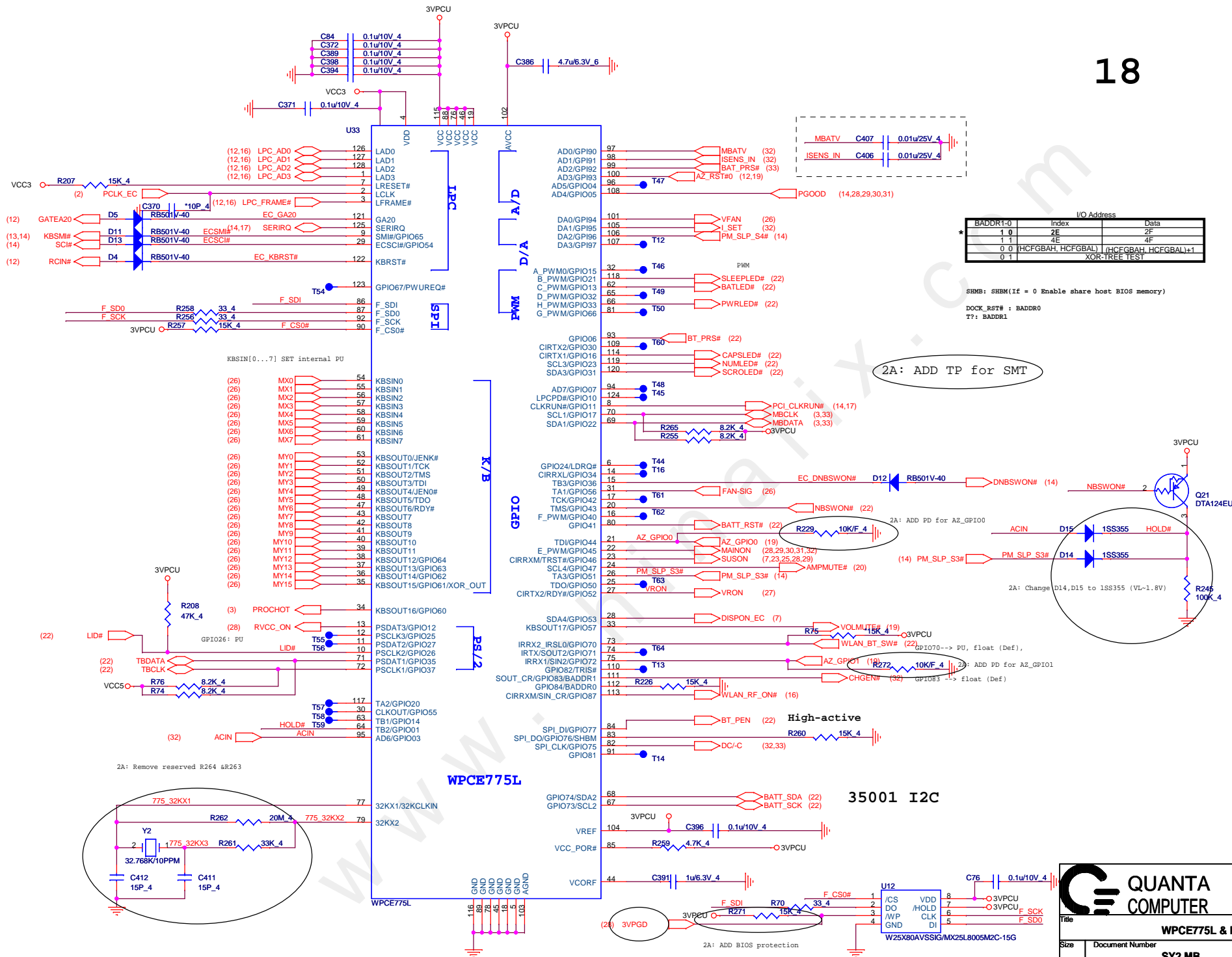
SY2 MB

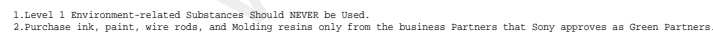
Rev	2C
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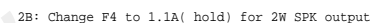
Date: Friday, April 10, 2009


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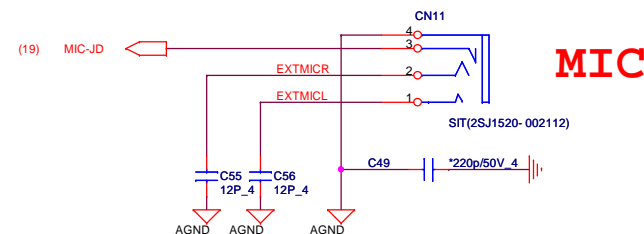
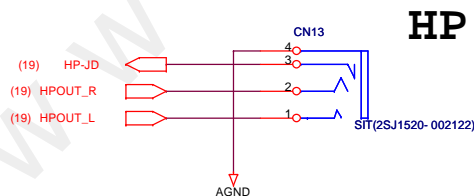
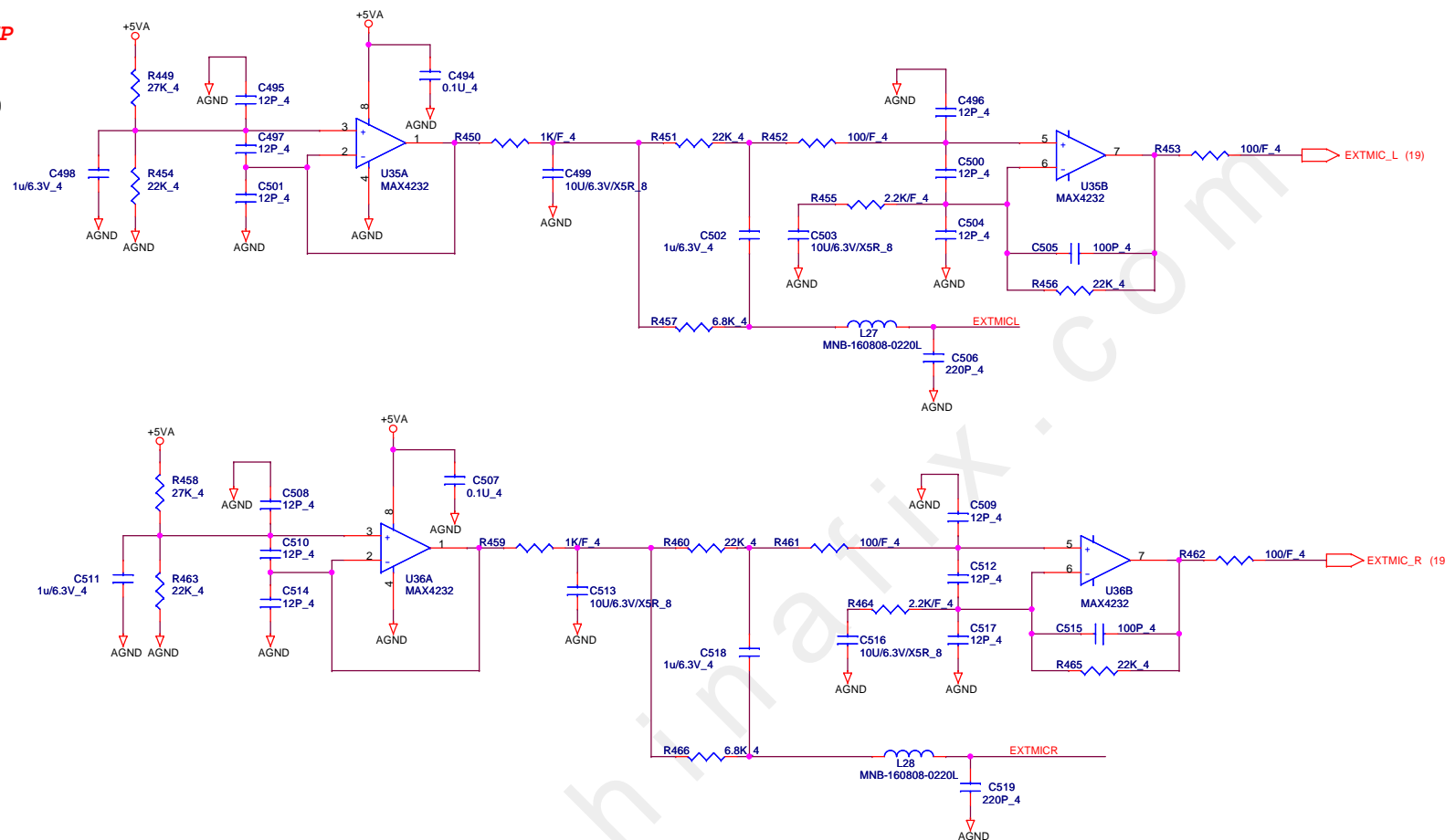


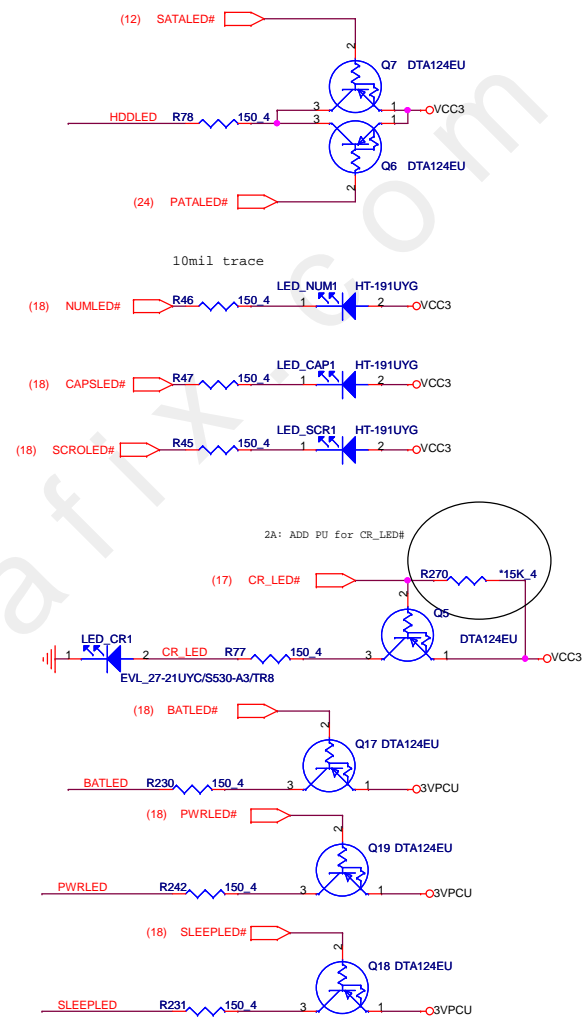


 <div> <div>QUANTA</div> <div>COMPUTER</div> </div>	
<div>Title</div> <div>AMP TPA2017D2</div>	
<div>Size</div> <div>Custom</div>	<div>Document Number</div> <div>SY2 MB</div>
<div>Date:</div> <div>Friday, April 10, 2009</div>	<div>Sheet</div> <div>20 of 36</div>

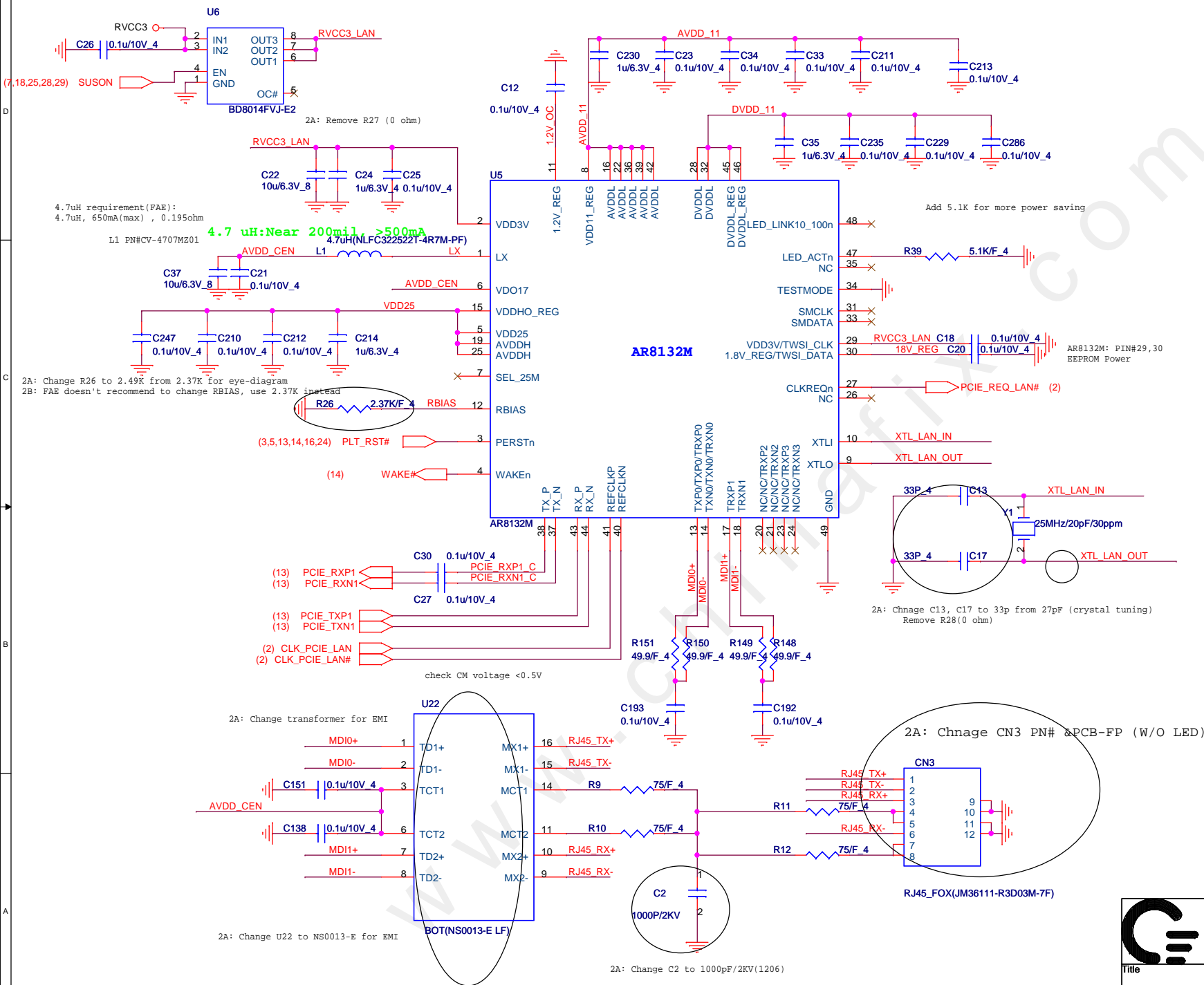
MIC Pre-AMP

2A: Change MIC- AMP circuit





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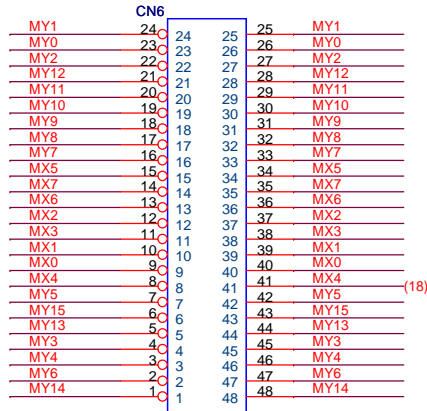
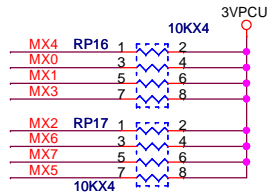
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Title			
LAN AR8132M			
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USB Connector

INT. KEYBOARD

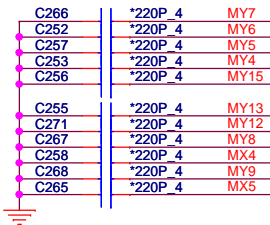
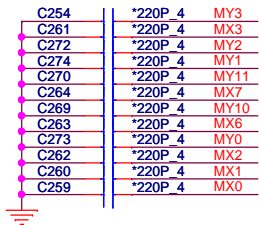
26



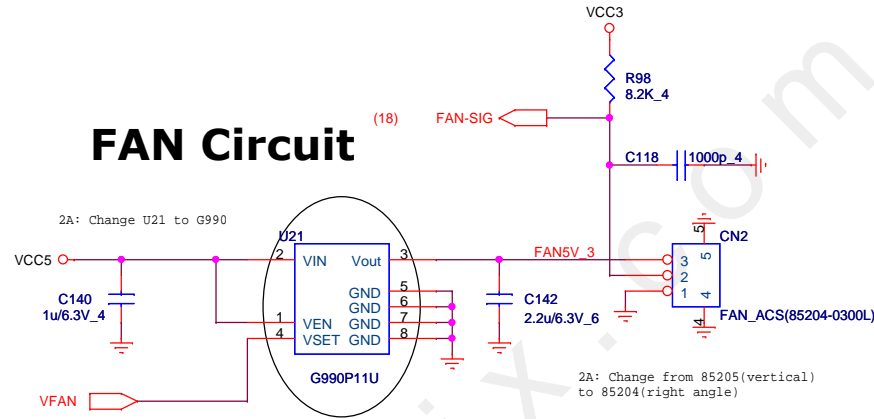
MX[0..7] >> MX[0..7] (18)
MY[0..15] >> MY[0..15] (18)

KB_ACS(88483-2401)

check internal PU



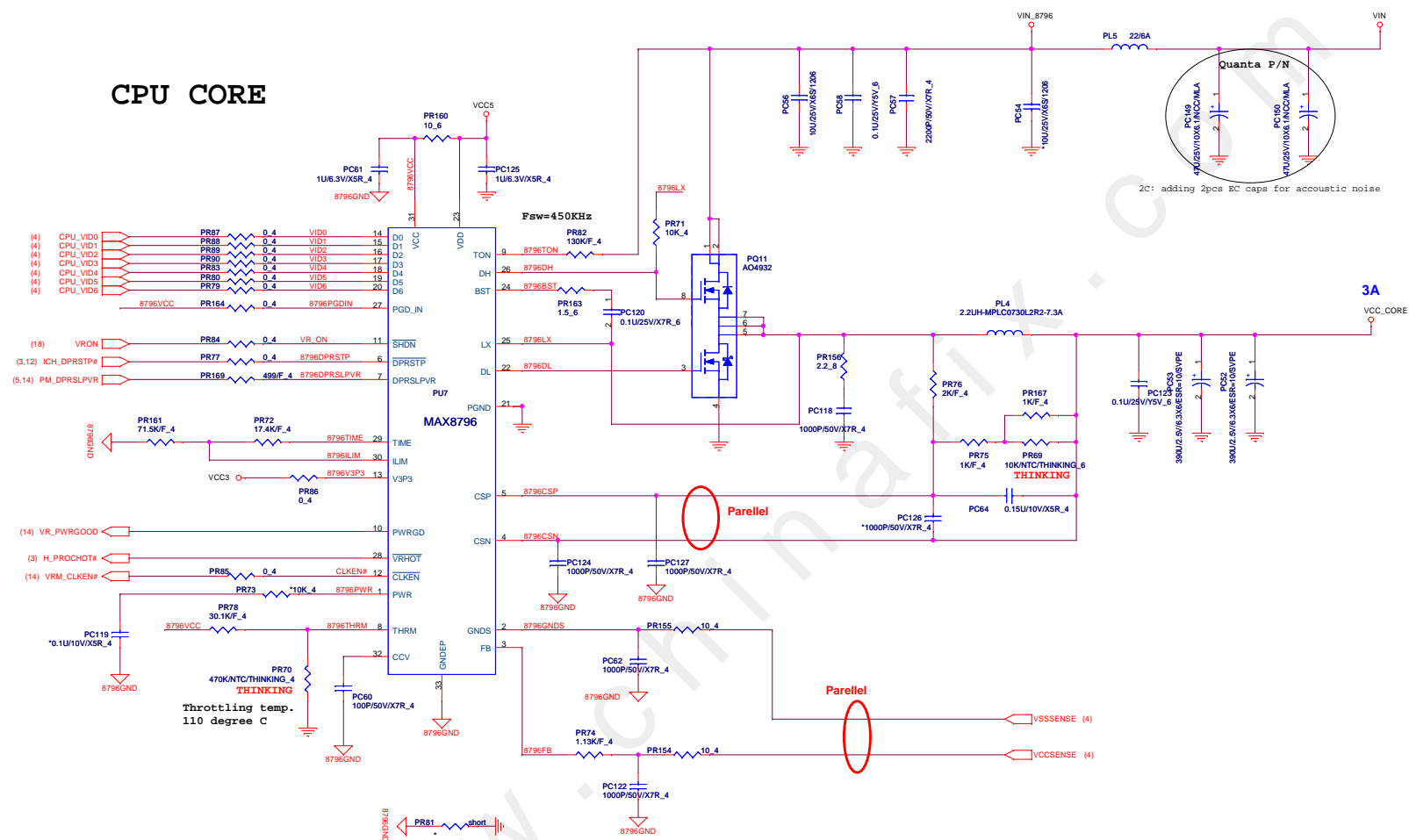
FAN Circuit

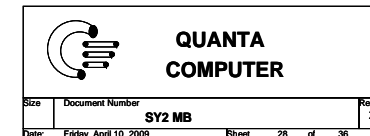


2A: Change from 85205(vertical) to 85204(right angle)

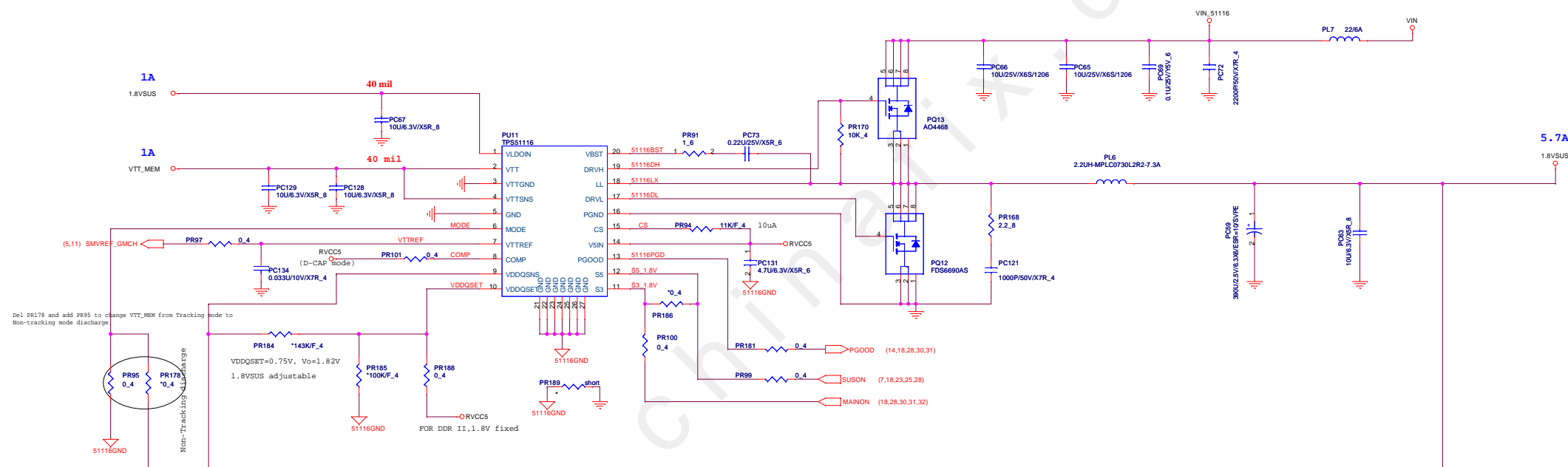
Title			
K/B, FAN, T/P			
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1.8VSUS & VTT_MEM



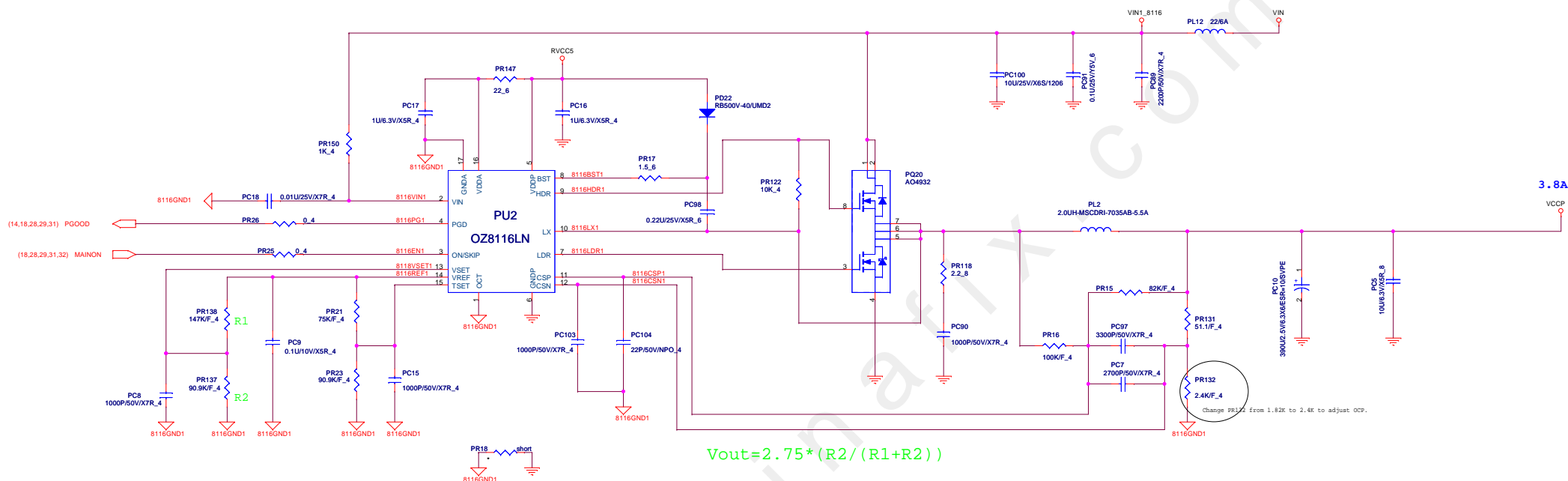
MODE	DISCHARGE MODE
+5V	No discharge
+1.8V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	2.5 fixed	VDDQSNS/2	DDR
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

VTT = VTTREF = VDDQSNS/2 = 0.9V

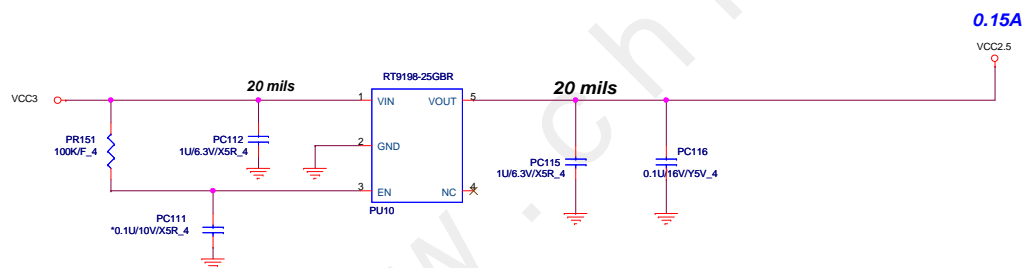
STATE	S3	S5	1.8VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

VCCP



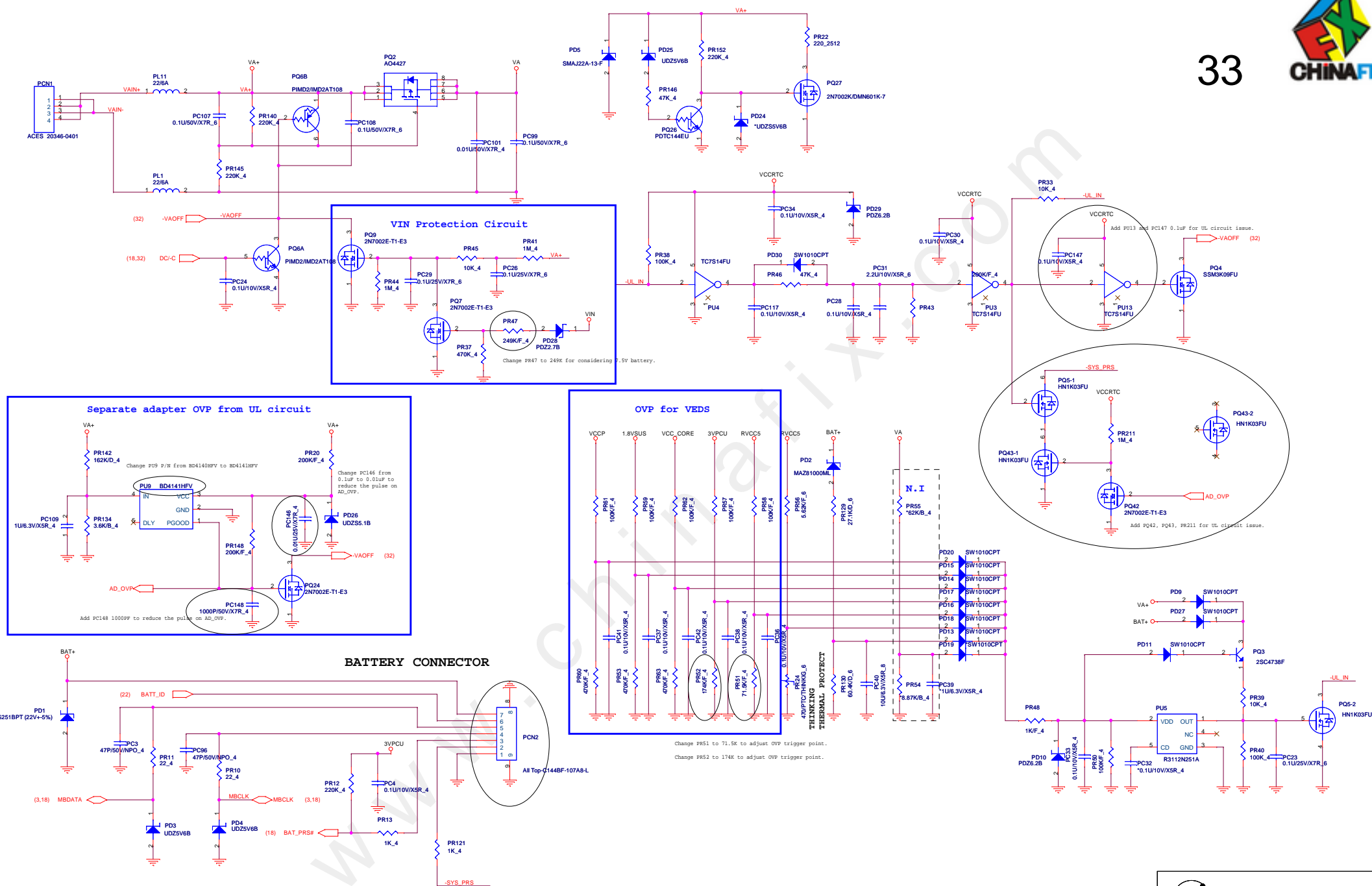
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VCC2.5

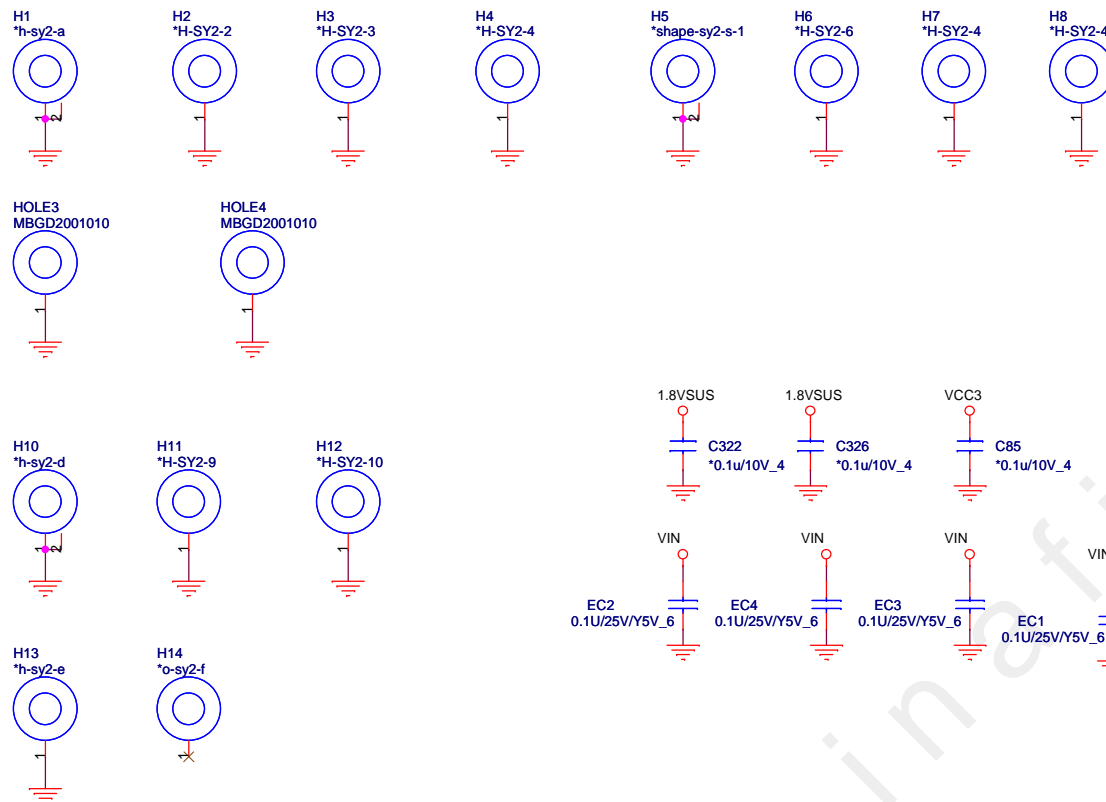





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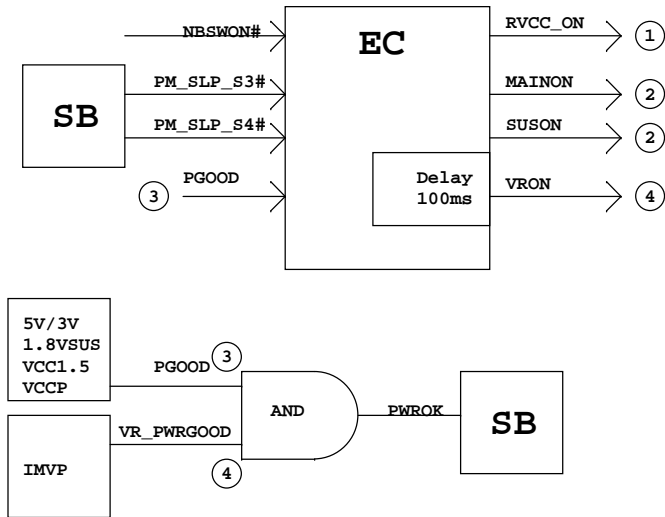
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Title Screw Hole			
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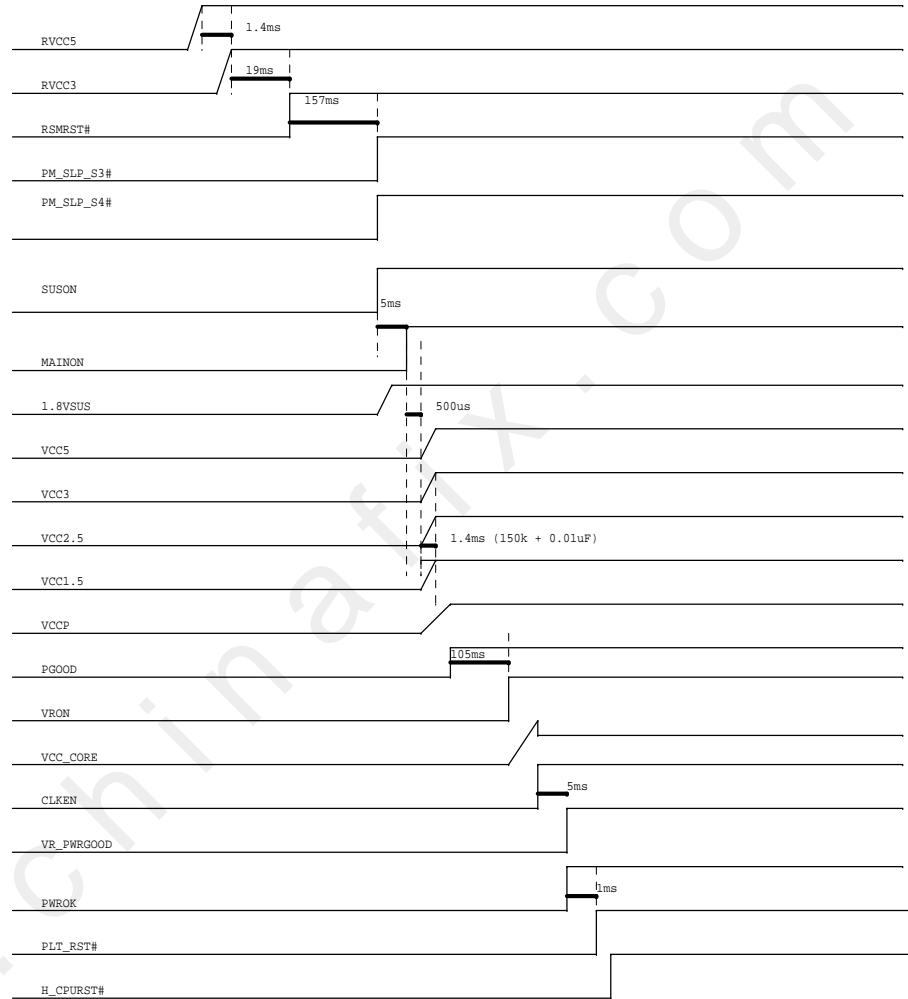
SY2 Power-up Block



Power State Table

AC Mode	S0	S3	S4	S5	BATT	S0	S3	S4	S5
6237LDO5	ON	ON	ON	ON	6237LDO5	ON	ON	ON	ON
3VPCU	ON	ON	ON	ON	3VPCU	ON	ON	ON	ON
RVCC5	ON	ON	ON	OFF	RVCC5	ON	ON	OFF	OFF
RVCC3	ON	ON	ON	OFF	RVCC3	ON	ON	OFF	OFF
1.8VSUS	ON	ON	OFF	OFF	1.8VSUS	ON	ON	OFF	OFF
VCC5	ON	OFF	OFF	OFF	VCC5	ON	OFF	OFF	OFF
VCC3	ON	OFF	OFF	OFF	VCC3	ON	OFF	OFF	OFF
VCC2.5	ON	OFF	OFF	OFF	VCC2.5	ON	OFF	OFF	OFF
VCCP	ON	OFF	OFF	OFF	VCCP	ON	OFF	OFF	OFF
VCC_CORE	ON	OFF	OFF	OFF	VCC_CORE	ON	OFF	OFF	OFF

SY2 Power-up Sequencing



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Title

Power-up Sequence

Size
B

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1219:(1A)
First release

1231:(1B)
-P.2
Modify CLK_FSC, CLK_FSB strapping circuit to CLK-GEN
Change PCI CLK damping to 22ohm (impedance matching)
-P.9
Reserve one 220uF for 1.8VSUS to 945GSE
-P.10
Change CRT-SCK, CRT-SDA PU to 2.2K for compatibility
Change DDC2BC, DDC2BD PU to 3.9K for compatibility
Change VCC5CRT circuit using fuse and Schottky
-P.14
Modify RSMRST# buffer circuit
-P.17
Change R5C833 GBRST# circuit
-P.20
Reserve 0 ohm to AMP R/L_in
Change AMP to APA2031
-P.21
Change fuse to 0.12A for Hall sensor
Change fuse to 0.12A for TP/B

0114(1C):
-P.7
Change CAMERA LDO to APL5151
-P.10
Change power of VCC_SYNC to VCC5CRT
Tie VGA CN#10 to GND
-P.14
ADD PU/PD for GPIO (default input)
-P.16
NC Wi-LAN WAKE# PIN#
Change WLAN_BT_LED circuit
-P.17
STUFF 1000p_4 for MS:CD#, SD: CD#, WP
Change MS/SD Power S/W to MAX1558H
-P.19
Connect Codec GPIO1 to EC for AMP standby
Change +5VA LDO to APL5151 for better PSRR

0119(1D)
-P.2
Reserve damping resistor for crystal
-P.10
Remove CRT PnP
-P.18
Remove CRTSENSE# to disable CRT PnP
Change AMPMUT# to PIN#24(OD type)
-P.21
Change BT PWR S/W to LDO
-P.32
Separate adapter OVP from UL circuit

0202(1E)
-P.7
Change CAMERA LDO to G909-330T1U(current limit>150mA)
Change LVDS PWR S/W to G5243A
-P.14
PU "ICH_RI#" to RVCC3
-P.17
Change R5C833 INTERRUPT to INTB#
-P.21
Move CR LED to MB from TP/B

0325(2A)
-P.2
Remove reserved 0ohm (R95,R106,R105)
-P7
Change C96 to 1uF for abnormal operation
Reserve L11 and C126 for EMI
-P9
Remove reserved L3-6, C3
Remove unnecessary C105
-P10
Change F3 to 0.25A ((hold)
Change CN7 PCB-FF
-P14
Change R168 to 332K (delay time-22ms)
Remove reserved SUSCLK
-P15
Remove reserved L2
-P16
Change D10 to RB501V-40
Remove reserved R125(0 ohm)
-P17
ADD C413-C416 for signal integrity
Change CN15.14 to WP (mistake)
Remove reserved R229 (0 ohm)
Move C402 near CN17
-P18
ADD BIOS protection circuit to
ADD PD for AZ_GPIO0 and AZ_GPIO1
Change D14,D15 to 1S8355 (VL-1.8V)
Remove reserved R263, R264
-P19
ADD L12 and reserved C124 for EMI
Change C376 to 0.01uF for G916
Change L10 to 1ohm
Add reserved C419 (10uF) for VCC5
-P20
Change C78,C81, C395, C397 to 0.47uF
for better Low freq response.
-P21
Change MIC- PREAMP circuit
-P22
Change U16 to G909-33 same as U17
ADD R237 and C400 for ESD
-P23
Change R26 to 2.49K for better PCIE eye
Change U6 to BD8014
Remove reserved R27 (0ohm)
Change C13 and C17 to 33pF (crystal tuning)
Change C2 to 1000p/2KV (1206 size)
Change U22 to NS013-E for EMI
-P24
Change F2 to 0.5A(Hold)
-P26
Change U21 to GMT G990
-P28
Remove PC143 for power up sequence
-P29
Mount PR96 and un-stuff PR178 for discharge mode
-P31
Cange PR64/PC46 to 150K/ 0.1u for power up sequence

0403 (2B)
-P4
Remove reserved C5
-P7
Change CN1 pin definition
-P12
Reserve R27 (0 ohm)
-P19
ADD C124 with 100pF for DMIC_CLK
ADD C361, C362 and reserve C520 and C521
-P20
Change F4 to 1.1A(hold) for 2W SPK
Change U34(AMP) to TPA2016D2
-P24
Change SSD FFC CNN to easy on type.
-P.27
Remove jumper PG3.
Remove PC55 due to PC55 is reserved only.
-P.28
Remove jumper PG5, PG6
-P17
Change PR173 from 143K to 174K to adjust OCP.
Del PR176 to enable No-audible skip mode for light load accoustic
noise improvement.
Del PC143 to adjust power sequence.
Separate 35VPGD to 3VPGD and 5VPGD respectively for EE request.
-P.29
Remove jumper PG4, PG8.
Del PR178 and add PR95 to change VTT_MEM from Tracking mode to
Non-tracking mode discharge.
-P.30
Remove jumper PG1.
Change PR132 from 1.82K to 2.4K to adjust OCP.
-P.31
Remove jumper PG2, PG7.
Change PR64 to 150K. Add PC46 0.01uF for power sequence.
-P.32
Change PR19 from 0.1 to 0.05 to adjust charge current to 1.5A
Add PC11 10uF to improve ripple/noise of the charger.
Change PR42 from 13K to 30K to adjust ACIN level.
-P.33
Add PUL3 and PC147 0.1uF for UL circuit issue.
Add PC149 1000PF to reduce the pulse on AD_OVP.
Change PC146 from 0.1uF to 0.01uF to reduce the pulse on AD_OVP.
Add PQ42, PQ43, PR211 for UL circuit issue.
Change PU9 P/N from BD4140HFV to BD4141HFV due to supplier change its
P/N.

0406A(2C)
-P.7
Change U17 to MAX4789
-P.9
Reserve L4,L5,L6
-P.15
Reserve L2
-P.19
Change R51 to connect AGND
-P.20
Change AMP(U37) to TPA2017D2
-P35
Update Power up sequence

0409 (2E)
-P.19
Connect R73 and Q3.1 to 3VPCU rather than RVCC5 for power down pop noise.
Change R220, R221,R224, R225 to 1.5K from 470ohm for POP-noise

0409 (2F)
-P.28
Add PR192, PR114, PC76 for PUL1 thermal protection.
Change PR191 to 130K for considering 7.5V battery.

0408 (2D)
-P.27
Add PC149, PC150 to improve accoustic noise.
-P.33
Change PR47 to 249K for considering 7.5V battery.
Change PR51 to 71.5K to adjust OVP trigger point.
Change PR52 to 174K to adjust OVP trigger point.

- 1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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